DC Biasing—BJTs

The following important basic relationships for a transistor:

$$V_{BE} = 0.7\ \text{V}$$

$$I_E = (\beta + 1)I_B \cong I_C$$

$$I_C = \beta I_B$$

For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated *Q*-point). Point *B* is a region of more linear spacing and therefore more linear operation, as shown inFig.1.Point B therefore seems the best operating point in terms of linear gain and largest possible voltage and current swing.

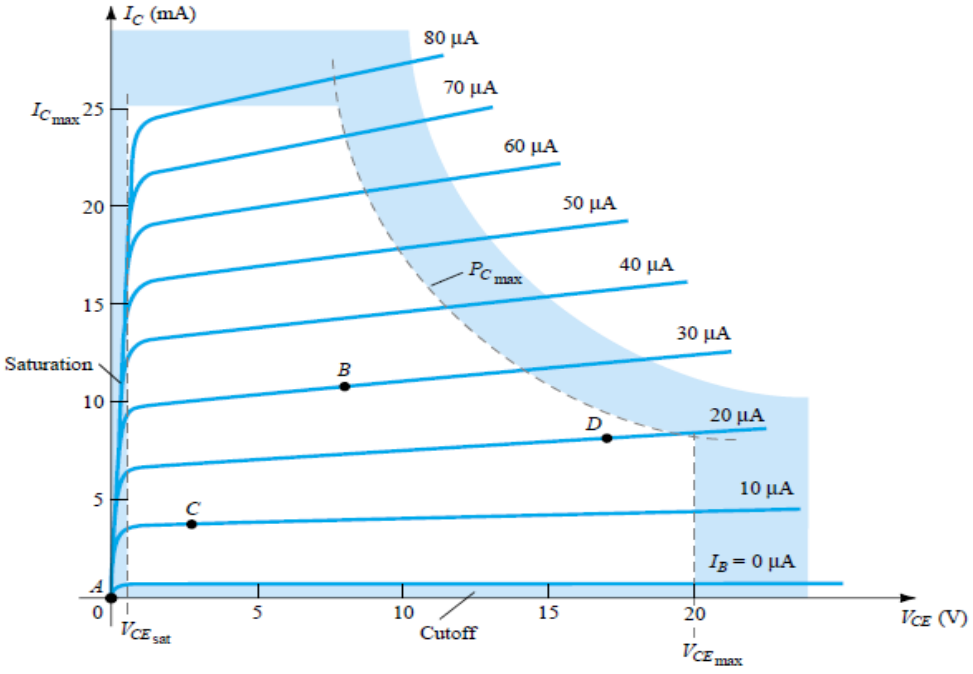


Fig.1: Various operating points within the limits of operation of a transistor

FIXED-BIAS CIRCUIT

In the Fig.2, for the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open circuit equivalent.

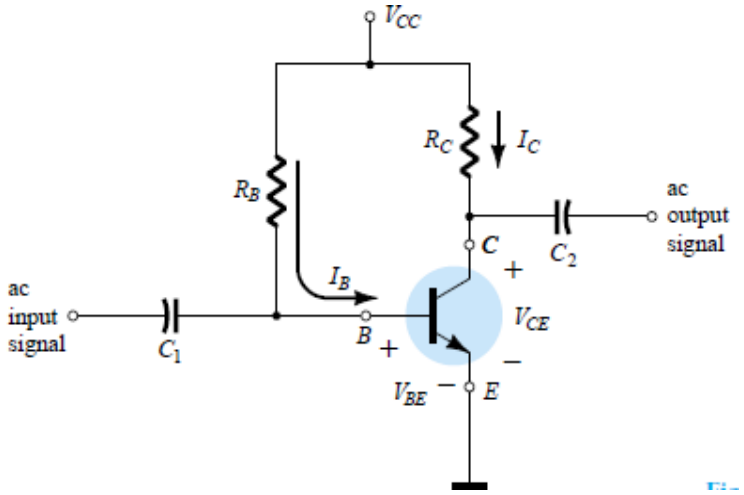


Fig.2: Fixed-bias circuit.

Forward Bias of Base–Emitter

Consider first the base–emitter circuit loop of Fig.3:a Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

Solving the equation for the current *IB* will result in the following

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

The selection of a base resistor, *RB*, sets the level of base current for the operating point.

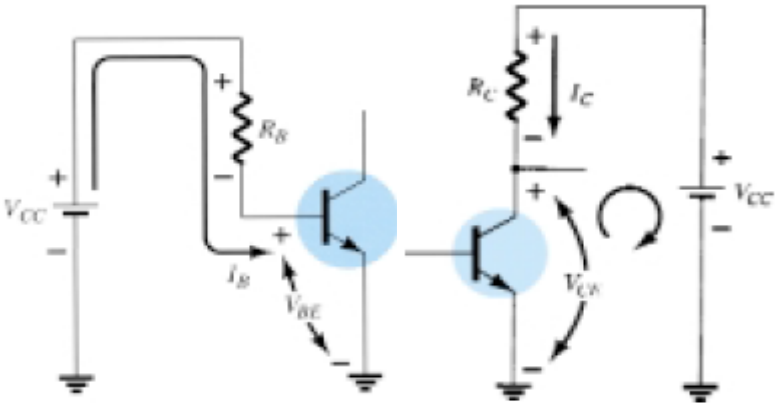


Fig.3:a: Base–emitter loop Fig.3:b: Collector–emitter loop

Collector–Emitter Loop

The magnitude of the collector current is related directly to *IB* through

$$I_C = \beta I_B$$

The level of $R_C$will determine the magnitude of V_{CE}, which is an important parameter. Applying Kirchhoff's voltage law in the clockwise direction around the indicated closed loop of Fig.3:bwill result in the following:

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

The saturation current is

$$\boxed{I_{C_{sat}} = \frac{V_{CC}}{R_C}}$$

Load-Line Analysis

The network of Fig.4:a establishes an output equation that relates the variables *IC* and *VCE* in the following manner:

$$\boxed{V_{CE} = V_{CC} - I_C R_C}$$

On the output characteristics is to use the fact that a straight line is defined by two points. If we *choose* $I_C$to be 0 mA, we are specifying the horizontal axis as the line on which one point is located. By substituting I_C=0 mA into Equation above, we find that

$$\boxed{V_{CE} = V_{CC}|_{I_C = 0\ \text{mA}}}$$

Defining one point is for the straight line as shown in Fig.5.If we now *choose* $V_{CE}$to be 0 V, which establishes the vertical axis as the line on which the second point will be defined, we find that *IC* is determined by the following equation:

$$0 = V_{CC} - I_C R_C$$

$$\boxed{I_C = \frac{V_{CC}}{R_C}\bigg|_{V_{CE} = 0\ \text{V}}}$$

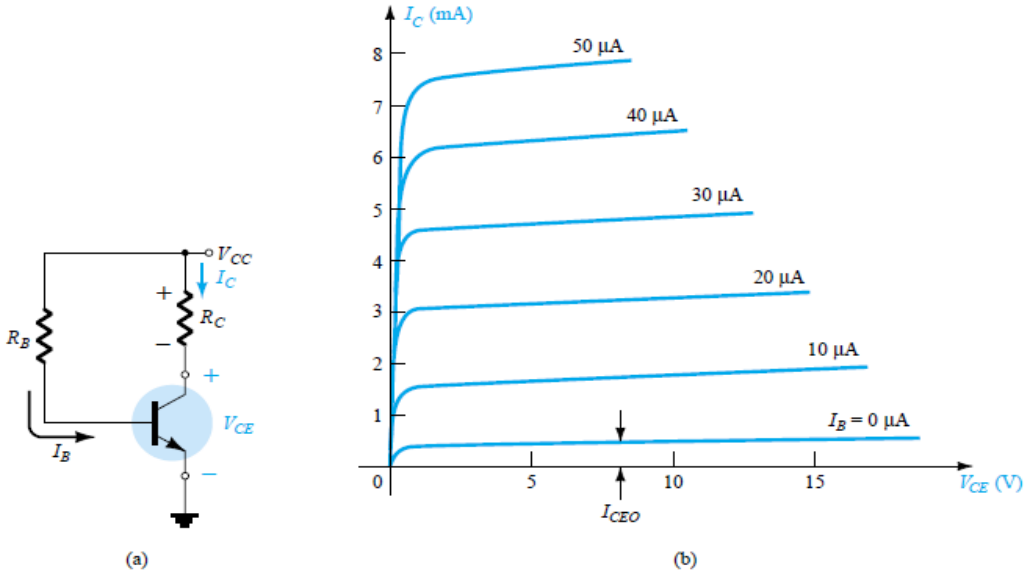


Fig.4: Load-line analysis: (a) the network; (b) the device characteristics.

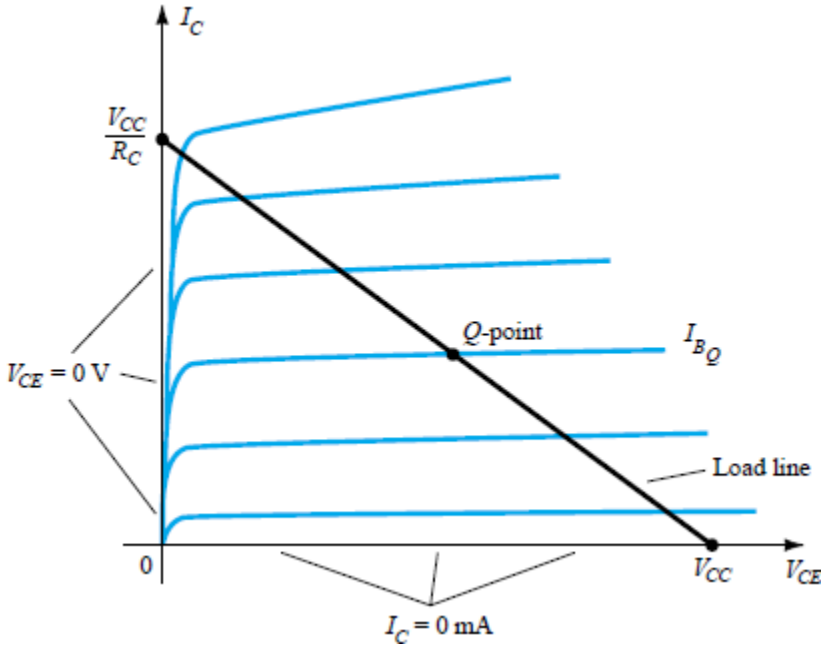


Fig.5: Fixed-bias load line.

The resulting line on the graph of Fig.5 is called the ***load line***since it is defined by the load resistor *RC*. By solving for the resulting level of I_B, the actual *Q*-point can be established as shown in Fig. 5.

If the level of *IB* is changed by varying the value of *RB* the *Q*-point moves up or down the load line as shown in Fig. 4.6. If *VCC* is held fixed and *RC* changed, the load line will shift as shown in Fig. 4.7. If *IB* is held fixed, the *Q*-point will move as shown in the same figure. If *RC* is fixed and *VCC* varied, the load line shifts as shown in Fig. 4.8.

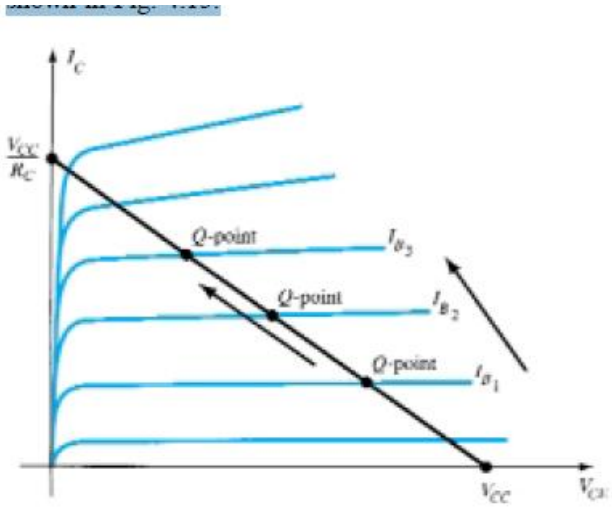


Fig.6 Movement of *Q*-point with increasing levels of *IB*.

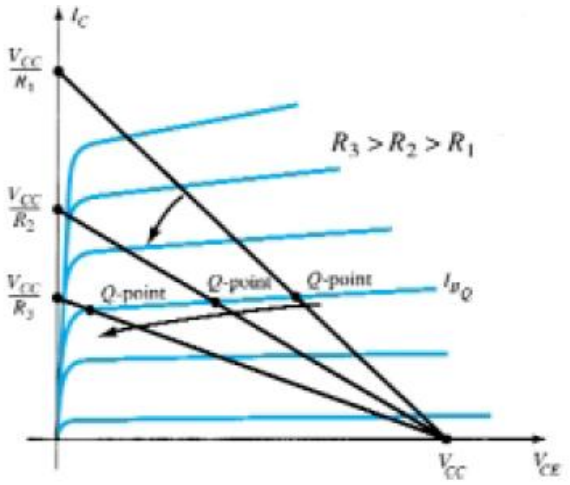


Fig.7 Effect of increasing levels of $R_C$on theload line and *Q*-point

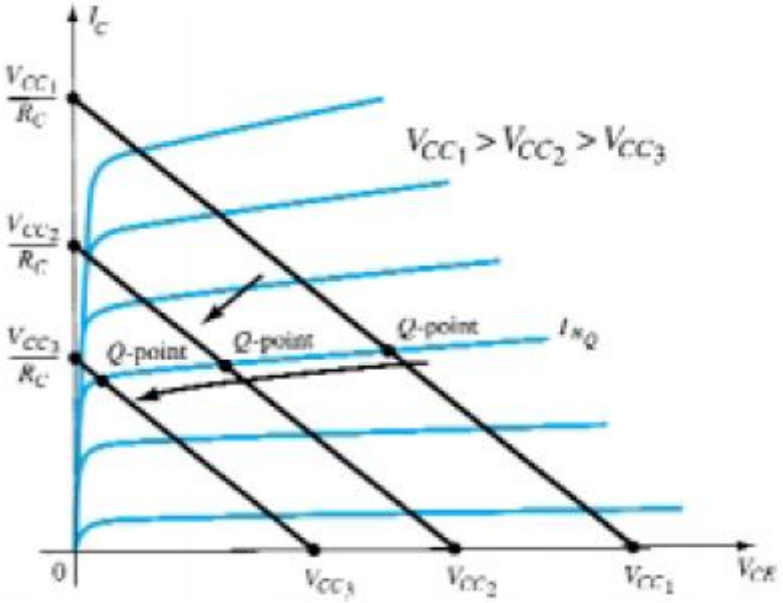


Fig.8: Effect of lower values of *VCC* on the load line and *Q*-point

Example: Given the load line of Fig. 4.9 and the defined *Q*-point, determine the required valuesof *VCC*, *RC*, and *RB* for a fixed-bias configuration.

$$V_{CE} = V_{CC} = \mathbf{20\ V} \text{ at } I_C = 0\ \text{mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0\ \text{V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20\ \text{V}}{10\ \text{mA}} = \mathbf{2\ k\Omega}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20\ \text{V} - 0.7\ \text{V}}{25\ \mu\text{A}} = \mathbf{772\ k\Omega}$$

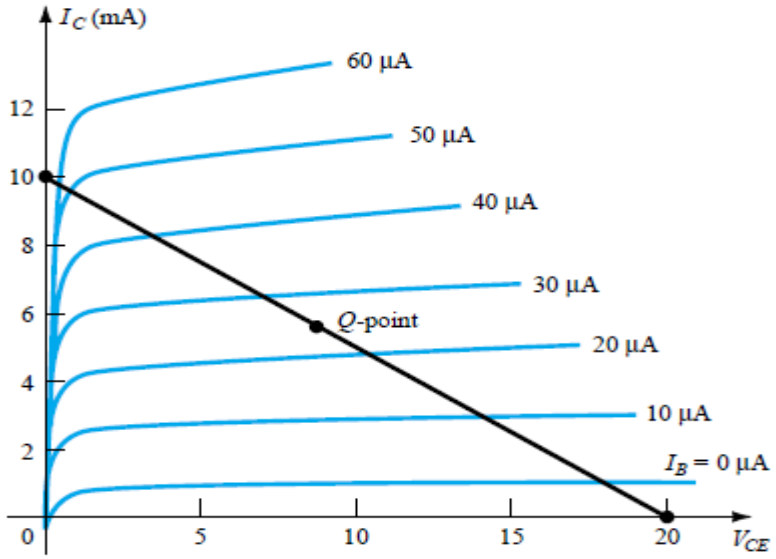


Fig.9 For example above

EMITTER-STABILIZED BIAS CIRCUIT

The dc bias network of Fig.4.10 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration.

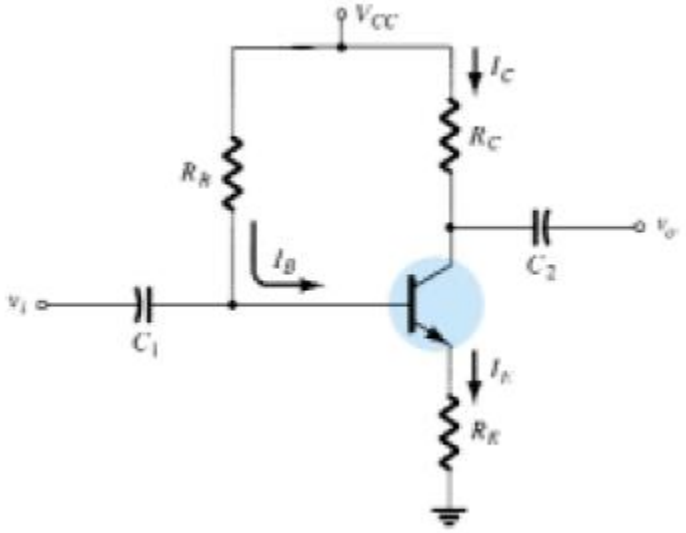


Fig.10: BJT bias circuit with emitter resistor.

Base–Emitter Loop

Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in the following equation:

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

As we know: $$I_E = (\beta + 1) I_B$$

Substituting for *IE*

$$V_{CC} - I_B R_B - V_{BE} - (\beta + I) I_B R_E = 0$$

Grouping terms will then provide the following:

$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

Multiplying through by (-1) we have

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

with

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

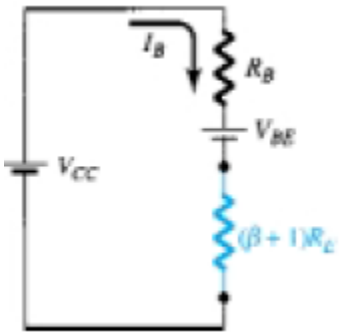
and solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

Note that the only difference between this equation for $I_B$and that obtained for the fixed-bias configuration is the term $(\beta+1)R_E$.

the case for the network of Fig. 4.11. Solving for the current I_B will result in the same equation obtained above. Since βis typically 50 or more, the emitter resistor appears to be a great deal larger in the base circuit. In general, therefore, for the configuration of Fig. 4.12.

$$R_i = (\beta + 1)R_E$$



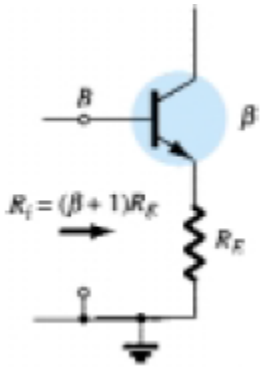


Fig.11: Network derived from Equation Fig.12: Reflected impedance level of R_E.

Collector–Emitter Loop

The collector–emitter loop is redrawn in Fig. 4.13. Writing Kirchhoff's voltage lawfor the indicated loop in the clockwise direction will result in:

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting $I_E \cong I_C$ and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

and

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

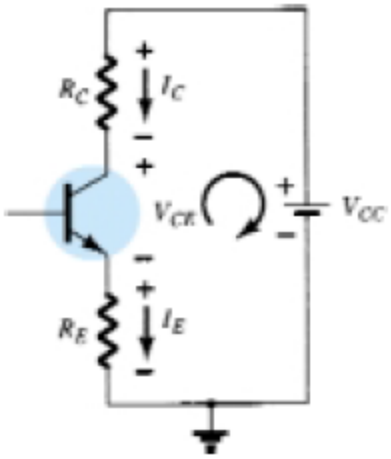


Fig. 13: Collector–emitter loop.

The single-subscript voltage *VE* is the voltage from emitter to ground and is determined by

$$V_E = I_E R_E$$

while the voltage from collector to ground can be determined from

$$V_{CE} = V_C - V_E$$

and

$$V_C = V_{CE} + V_E$$

or

$$V_C = V_{CC} - I_C R_C$$

The voltage at the base with respect to ground can be determined from

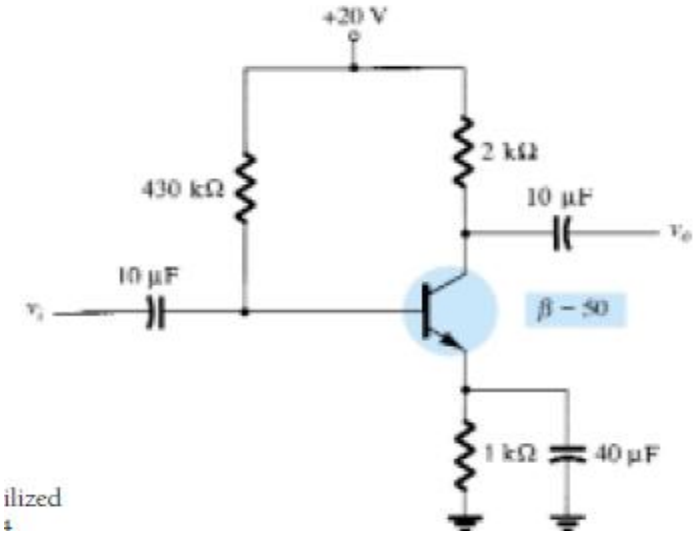
$$V_B = V_{CC} - I_B R_B$$

or

$$V_B = V_{BE} + V_E$$

EXAMPLE 4.4: For the emitter bias network of Fig. 4.14, determine:

a) I_B, b) I_C, c)V_{CE}, d)V_C, e)V_E, f)V_B, g)V_{BC}



ilized

Fig.14

Solution:

(a) Eq. (4.17): $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{430\text{ k}\Omega + (51)(1\text{ k}\Omega)}$$
$$= \frac{19.3\text{ V}}{481\text{ k}\Omega} = \mathbf{40.1\ \mu A}$$

(b) $$I_C = \beta I_B$$
$$= (50)(40.1\ \mu\text{A})$$
$$\cong \mathbf{2.01\ mA}$$

(c) Eq. (4.19): $$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega + 1\text{ k}\Omega) = 20\text{ V} - 6.03\text{ V}$$
$$= \mathbf{13.97\ V}$$

(d) $$V_C = V_{CC} - I_C R_C$$
$$= 20\text{ V} - (2.01\text{ mA})(2\text{ k}\Omega) = 20\text{ V} - 4.02\text{ V}$$
$$= \mathbf{15.98\ V}$$

(e) $$V_E = V_C - V_{CE}$$
$$= 15.98\text{ V} - 13.97\text{ V}$$
$$= \mathbf{2.01\ V}$$

or $$V_E = I_E R_E \cong I_C R_E$$
$$= (2.01\text{ mA})(1\text{ k}\Omega)$$
$$= \mathbf{2.01\ V}$$

(f) $$V_B = V_{BE} + V_E$$
$$= 0.7\text{ V} + 2.01\text{ V}$$
$$= \mathbf{2.71\ V}$$

(g) $$V_{BC} = V_B - V_C$$
$$= 2.71\text{ V} - 15.98\text{ V}$$
$$= \mathbf{-13.27\ V}\quad \text{(reverse-biased as required)}$$

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals.

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor

EXAMPLE 4.6: Determine the saturation current for the network of Example 4.4.

$$I_{C_{sat}} = \frac{V_{CC}}{R_C + R_E}$$

$$= \frac{20\text{ V}}{2\text{ k}\Omega + 1\text{ k}\Omega} = \frac{20\text{ V}}{3\text{ k}\Omega}$$

$$= \mathbf{6.67\text{ mA}}$$

which is about twice the level of $I_{CQ}$for Example 4.4.

Load-Line Analysis

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration.

The collector–emitter loop equation that defines the load line is the following:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Choosing $I_C = 0$ mA gives

$$\boxed{V_{CE} = V_{CC}\big|_{I_C=0\text{ mA}}}$$

as obtained for the fixed-bias configuration. Choosing $V_{CE} = 0$ V gives

$$\boxed{I_C = \frac{V_{CC}}{R_C + R_E}\bigg|_{V_{CE}=0\text{ V}}}$$

As shown in Fig. 15. Different levels of *IBQ* will, of course, move the *Q*-point up or down the load line.

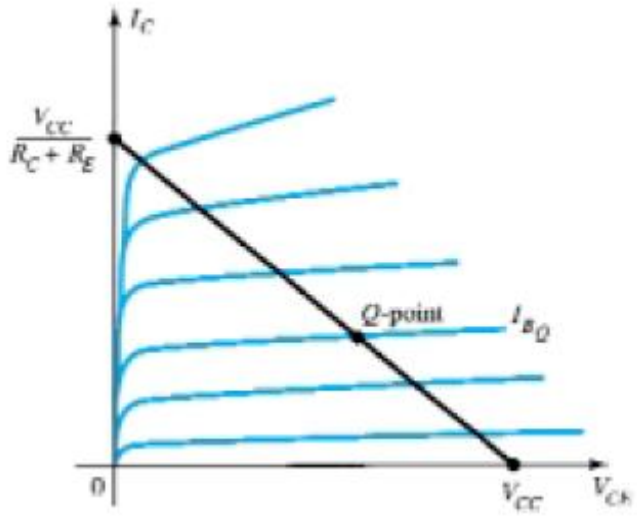
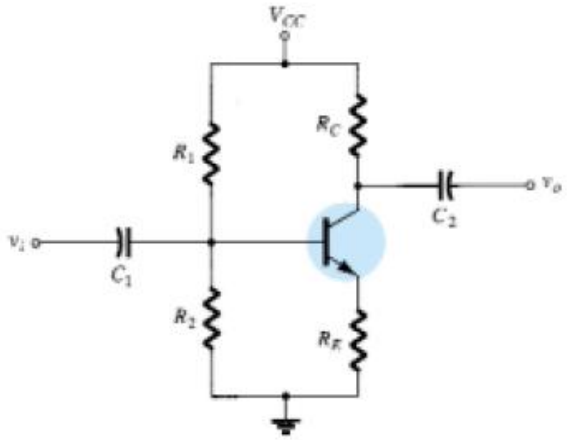


Fig. 15: Load line for the emitter-bias configuration

VOLTAGE-DIVIDER BIAS

The bias current $I_{CQ}$and voltage V_{CEQ}were a function of the current gain (β) of the transistor.

sinceβ is temperature sensitive



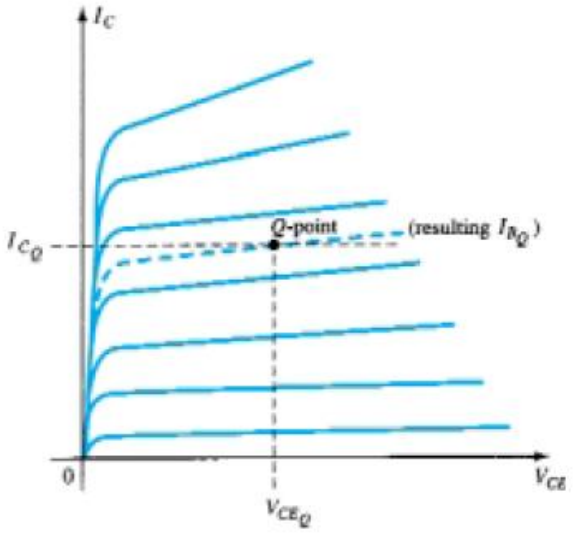


Fig.16: Voltage-divider bias configuration.Fig. 17:Defining the *Q*-point for the voltage-divider bias configuration.

There are two methods that can be applied to analyze the voltage divider configuration.The ***exact method***can be applied to *any* voltage-divider configuration. The second is referredto as the ***approximate method***and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a **savings in time and energy**.

Exact Analysis

The input side of the network of Fig.16 can be redrawn as shown in Fig.18. The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

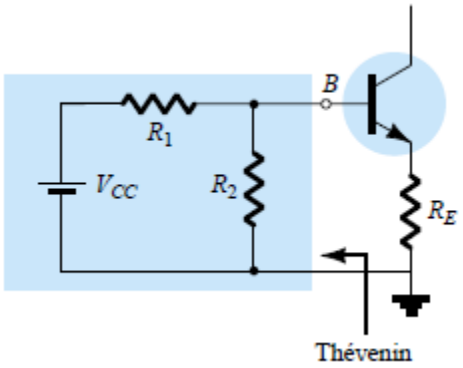


Fig.18: Redrawing the input side of the network of Fig. 16.

***R_{th}*:** The voltage source is replaced by a short-circuit equivalent

$$R_{\text{Th}} = R_1 \| R_2$$

$$E_{\text{Th}} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

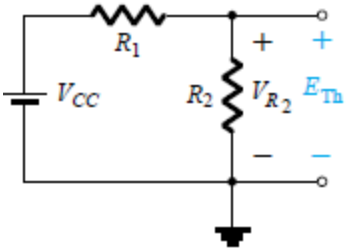


Fig.19: Determining E_{Th}

I_{BQ}can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:

$$E_{\text{Th}} - I_B R_{\text{Th}} - V_{BE} - I_E R_E = 0$$

Substituting $I_E = (\beta + 1)I_B$ and solving for I_B yields

$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E}$$

Once $I_B$is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

EXAMPLE 4.7: Determine the dc bias voltage *VCE* and the current *IC* for the voltage-divider configuration of Fig. 4.20

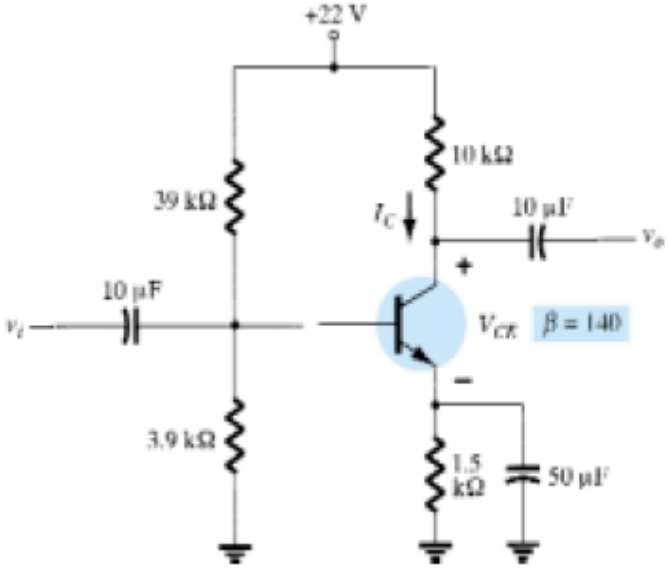


Fig.20: Beta-stabilized circuit for Example 4.7.

$$R_{\text{Th}} = R_1 \| R_2$$

$$= \frac{(39\ \text{k}\Omega)(3.9\ \text{k}\Omega)}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega} = 3.55\ \text{k}\Omega$$

$$E_{\text{Th}} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= \frac{(3.9\ \text{k}\Omega)(22\ \text{V})}{39\ \text{k}\Omega + 3.9\ \text{k}\Omega} = 2\ V$$

$$I_B = \frac{E_{\text{Th}} - V_{BE}}{R_{\text{Th}} + (\beta + 1)R_E}$$

$$= \frac{2\ \text{V} - 0.7\ \text{V}}{3.55\ \text{k}\Omega + (141)(1.5\ \text{k}\Omega)} = \frac{1.3\ \text{V}}{3.55\ \text{k}\Omega + 211.5\ \text{k}\Omega}$$

$$= 6.05\ \mu A$$

$$I_C = \beta I_B$$

$$= (140)(6.05\ \mu\text{A})$$

$$= \mathbf{0.85\ mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 22\ \text{V} - (0.85\ \text{mA})(10\ \text{k}\Omega + 1.5\ \text{k}\Omega)$$

$$= 22\ \text{V} - 9.78\ \text{V}$$

$$= \mathbf{12.22\ V}$$